- * Indicates the instruction will only execute if the Status Bit is TRUE (ON)
- All test inputs, AND's, OR's, will effect the Status Bit.
- Last update 1/10/05

INSTR	OP CODE	INSTR	OP CODE SB	DESCRIPTION
TIH	1000			Test input on hi level, SB true/false
TIL	1400			Test input on lo level, SB true/false
TFH	3000			Test flag on hi level, SB true/false
TFL	3400			Test flag on lo level, SB true/false
AIH	0000			AND input on hi level, SB true/false
AIL	0400			AND input on lo level, SB true/false
AFH	2000			AND flag on hi level, SB true/false
AFL	2400			AND flag on lo level, SB true/false
OIH	0800			OR input on hi level, SB true/false
OIL	0C00			OR input on lo level, SB true/false
OFH	2800			OR flag on hi level, SB true/false
OFL	2C00			OR flag on lo level, SB true/false
(M)=0	1800			Test contents of memory equals zero
	MA			Memory Address
((M))=0	F800			Test contents of contents of memory = 0
	MA			Memory Address
SBN	1C00			Set status bit on
SBF	1C01			Set status bit off
SOF	4000	SOF*	4400	Set Output Off
SON	4800	SON*	4C00	Set Output On
TNW	3800	TNW*	3C00	Timer on contents of memory
MA		MA		Memory Address
T(M)	9800	T(M)*	9C00	Timer on contents of contents of memory
MA		MA		Memory Address
T((M))	D800	T((M))*	DC00	Timer on contents of contents of contents of
MA		MA		memory. Memory Address
JNW	5000	JNW*	5400	Jump to contents of next word.
MA		MA		Memory Address
J(M)	5800	J(M)*	5C00	Jump to contents of memory.
MA		MA		Memory Address
(M)C	6000	(M)C*	6400	Load contents of memory into CRU
MA		MA		Memory Address
((M))C	B000	((M))C*	B400	Load contents of contents of memory to CRU
MA		MA		Memory Address
(C)M	6800	(C)M*	6C00	Load contents of CRU into memory

MA		MA		Memory Address
(C)(M) MA	B800	(C)(M)* MA	BC00	Load contents of CRU into contents of contents of memory. Memory Address
(M)R MA	8000	(M)R* MA	8400	Load contents of memory to Register Memory Address
((M))R MA	A000	((M))R* MA	A400	Load contents of contents of memory to Register. Memory Address
(R)M MA	8800	(R)M* MA	8C00	Load contents of register to memory Memory Address
(R)(M) MA	A800	(R)(M)* MA	AC00	Load contents of register to contents of contents of memory. Memory Address
NWM DATA MA	9000	NWM* DATA MA	9400	Load next word into memory Data Memory Address
NW(M) DATA MA	D000	NW(M)* DATA MA	D400	Load next word into contents of contents of memory. DATA Memory address
(M)+1 MA	7000	(M)+1* MA	7400	Increment contents of memory by 1 Memory Address
((M))+1 MA	C000	((M))+1* MA	C400	Increment contents of contents of memory by 1 Memory Address
(M)-1 MA	7800	(M)-1* MA	7C00	Decrement contents of memory by 1 Memory Address
((M))-1 MA	C800	((M))-1* MA	CC00	Decrement contents of contents of memory by 1
NOP	FFFF			No Operation